CLAIMS

What is claimed is:

1. A method for circuit modification of a microelectronic chip comprising at least one conductor in an organic dielectric, said method comprising:

applying a protective inorganic surface layer on said organic dielectric;

forming at least one window in said protective inorganic surface layer to selectively expose an underlying portion of said organic dielectric;

etching said organic dielectric in an area of said at least one window to selectively remove said organic dielectric adjacent to said at least one conductor; and

performing at least one process that modifies said at least one conductor.

2. The method in claim 1, wherein said modification process to said at least one conductor comprises at least one of:

milling said conductor with a focused ion beam;

milling said conductor with a focused ion beam in the presence of a passivating gas; and

depositing additional conductor material.

3. The method in claim 1, wherein said etching of said organic dielectric comprises a reactive ion etching.

4. The method in claim 1, wherein said at least one conductor comprises metal.

5. The method in claim 4, wherein said metal comprises copper.

6. The method in claim 1, wherein said protective inorganic surface layer includes an inorganic layer which etches selectively to the organic dielectric.

7. The method in claim 6, wherein said inorganic layer comprises nitride.

8. The method in claim 1, wherein said window is formed by a focused ion beam.

9. The method in claim 1, wherein said window is formed by a mask/resist process.

10. The method in claim 3, wherein said reactive ion etching uses one of oxygen and an oxygen compound.

11. The method in claim 2, wherein said passivation gas comprises xenon diflouride.

12. A method of selectively removing organic dielectric adjacent to a conductor, said method comprising:

depositing a protective inorganic surface layer onto said organic dielectric;

forming at least one window in said protective inorganic surface layer to selectively expose an underlying portion of said organic dielectric; and

etching said organic dielectric in an area of said at least one window to selectively remove said organic dielectric adjacent to said conductor.

13. The method of claim 12, wherein said etching comprises a reactive ion etching.

14. A method of manufacturing an electronic device having at least one layer of organic dielectric, said method comprising:

depositing a protective inorganic surface layer onto said at least one layer of organic dielectric;

forming at least one window in said protective inorganic surface layer to selectively expose an underlying portion of said organic dielectric; and

etching said organic dielectric in an area of said at least one window to selectively remove said organic dielectric.

15. The method of claim 14, wherein said etching comprises a reactive ion etching.

16. The method of claim 1, wherein said at least one conductor to be modified and said organic layer to be selectively removed are buried below at least one upper layer and

said method further comprises successively providing an opening in each of said at least one upper layer.

17. The method of claim 16, wherein said at least one of said at least one upper layer contains a second conductor obstructing said window area, and said method further comprises providing an opening in said second conductor.

18. A method for circuit modification of a microelectronic chip comprising at least one conductor embedded in an organic dielectric layer, said method comprising:

applying a protective inorganic layer onto a surface of said organic dielectric layer, such that said protective layer is contiguous to said organic layer;

opening at least one window in said protective inorganic layer to selectively expose an underlying portion of said organic dielectric; and

performing at least one process that modifies said a first conductor of said at least one conductor.

19. The method of claim 18, further comprising:

etching said organic dielectric in an area of said at least one window to selectively remove said organic dielectric adjacent to said first conductor of said at least one conductor.

20. The method of claim 18, further comprising:

etching an opening in an underlying protective layer to gain access to a second conductor located below said first conductor of said at least one conductor.

21. The method of claim 18, wherein said process that modifies said first conductor of said at least one conductor comprises providing an opening in said first conductor, and said method further comprising:

etching an opening in an underlying protective layer to gain access to a second conductor located below said first conductor of said at least one conductor.

22. A method of selectively removing organic dielectric on a microelectronic chip comprising:

depositing an inorganic surface layer on top of and contiguous to said organic dielectric;

forming at least one window in said inorganic surface layer to selectively expose an underlying portion of said organic dielectric; and

etching said organic dielectric in an area of said at least one window, thereby selectively removing said organic dielectric.

23. The method of claim 22, wherein said step of etching said organic dielectric comprises a reactive ion etching.

24. The method of claim 23, wherein said reactive ion etching uses one of oxygen and an oxygen compound.

25. A method of selectively removing organic dielectric on a microelectronic chip comprising the steps of:

a step of providing a protective inorganic surface layer on top of said organic dielectric;

a step of providing at least one opening in said protective inorganic surface layer to selectively expose the underlying said organic dielectric; and

a step of etching said organic dielectric in said at least one opening.

26. The method of claim 25, wherein said step of etching said organic dielectric comprises a reactive ion etching.

27. The method in claim 26, wherein said reactive ion etching uses one of oxygen and an oxygen compound.

28. A method of selectively removing, in a microelectronic chip, an organic dielectric adjacent to a conductor prior embedded in said layer prior to modifying said conductor, said method comprising:

etching said organic dielectric using reactive ion etching.

29. A method of repairing a microelectronic chip containing at least one conductor, said method comprising:

selectively removing dielectric material adjacent to said conductor prior to performing a procedure that modifies said conductor.

30. The method of claim 29, wherein said layer comprises an organic dielectric layer and said selective removal of adjacent dielectric material comprises reactive ion etching.

31. A method of performing circuit modifications having multiple levels of conductors embedded in respective multiple layers of organic dielectric, comprising:

providing at least one first opening through all overlying layers to expose said first organic layer;

etching said first organic layer through opening in overlying layers using reative ion etching;

etching through a first underlying isolation layer to expose a second organic layer.

32. A method of performing circuit modifications having multiple levels of conductors embedded in respective multiple layers of organic dielectric, at least one of said multiple layers containing a first conductor that obstructs a work area for a target second

conductor located in a second lower level organic dielectric layer, said method comprising:

providing at least one first opening through all overlying layers to expose said first organic layer containing said first conductor;

etching through said first conductor an opening sufficient to create a work area for said underlying target conductor;

etching through a first underlying isolation layer to expose any underlying layers separating said first organic layer from said second organic layer containing said target conductor, and etching through said separating layers; and

etching second organic layer to selectively remove organic dielectric adjacent to said target conductor using reactive ion etching.

33. A method of performing circuit modifications having multiple levels of conductors embedded in respective multiple layers of organic dielectric, a first surface organic dielectric layer containing a first conductor that obstructs a work area for a target second conductor located in a second lower level organic dielectric layer, said method comprising:

applying a first protective inorganic or mask layer;

providing an opening through said first protective inorganic or mask layer over target conductor;

through this opening, etching said first conductor an opening sufficient to create a work area for said underlying target conductor;

etching through a first underlying isolation layer to expose any underlying layers separating said first organic layer from said second organic layer containing said target conductor, and etching through said separating layers; and

etching second organic layer using a reactive ion etching to selectively remove organic dielectric adjacent to said first conductor.